ABSTRACT OF THE DISCLOSURE

A semiconductor testing circuit being arranged for testing a semiconductor storage device, and having a simple construction and a great number of executable test patterns. Counters designate portions of a write/read address by count values outputted from the counters, respectively, where each of the portions is comprised of one bit or a plurality of successive bits. A switching circuit selectively outputs counter-control signals for individually controlling operations of the counters. Each of the counter-control signals is a common counter-control signal commonly used for the counters or the most significant bit of one of the portions outputted from a first one of the counters other than a second one of the counters for which the counter-control signal is outputted. Thus, it is possible to change assignment of the write/read address to the count values of the counters.